

ANNA UNIVERSITY COIMBATORE

B.E/B.TECH. DEGREE EXAMINATIONS: MAY/JUNE 2010

REGULATIONS: 2008

FOURTH SEMESTER: EEE

080280029-DIGITAL LOGIC CIRCUITS

TIME: 3 Hours

Max.Marks:100

PART-A

(20*2=40 MARKS)

ANSWER ALL QUESTIONS

1. Convert 1110011 into hexa decimal.
2. Add (1A8)₁₆ and (67B)₁₆.
3. Express the Boolean function $F=xy+x'y$ as a product of max terms.
4. State Demorgan's theorem.
5. Differentiate combinational and sequential circuits.
6. Convert JK Flip Flop to D Flip Flop.
7. Draw the state diagram of JK flip flop.
8. A counter has 14 stable states 0000 through 1101. If the input frequency is 50 kHz, what will be the output frequency?
9. What is the difference between Hazard and Race?
10. Differentiate combinational and sequential circuits.
11. The Input frequency of a 4 bit ripple counter is 256 Hz. what is the output frequency?
12. Define Propagation delay.
13. What is open collector output TTL? Where is it used?
14. Expand FPGA. Give an example of such device.
15. Create a PLD description for a 3×8 MUX.
16. What do you mean by transition race and output race?
17. List the operators used in VHDL.
18. Define VHDL.

19. Write the VHDL code for binary divider.
20. Explain compilation and simulation of VHDL code.

PART-B

(5*12=60 marks)

ANSWER ANY FIVE QUESTIONS

21. Reduce the given function in both SOP and POS forms and design the circuit
 $F = \text{Sum}(0,2,3,4,6,7,8,12,14,15,16,18,19,20,22,23,24,28)$ (12)
- 22 (a). Implement $Y=ABCD$ using two input NAND gates (6)
- (b). Implement the combinational function using 8×1 multiplexer. (6)
- $$Y = AB + A'CD' + B'CD'$$
- 23 (a). Draw and explain the working of clocked RS Flip flop. (6)
- (b). Define a Latch? Explain D Latch with the timing Diagram. (6)
24. Design a sequential circuit with 4 JK Flip-Flops ABCD, the next states of B, C, D are equal to the present states of A, B,C. The next state of A is equal to the EX-OR of the Present states of C and D. (12)
25. Design a fundamental Asynchronous Sequential Network which has two inputs X1 and X2 and a single output Z to meet the following requirements.
1. The inputs X1 and X2 never change or are 1 simultaneously. (6)
 2. An output of $Z=1$ occurs only during the input state $X1X2 = 01$ and if and only if the input state $X1X2 = 01$ is preceded by the input sequence $X1X2=01, 00,10,00,10,00$. (6)
- 26 (a). Explain how EPROM can be used to realize a sequential circuit. (6)
- (b). Compare the operations of PLA and PAL devices using logic diagrams. (6)
- 27 (a). Distinguish between EPROM and EEPROM. (6)
- (b) Explain the various steps involved in writing a program into EPROM. (6)
28. Describe the modeling of
1. Flip flops using VHDL (6)
 2. Sequential Machine using VHDL. (6)

*****THE END*****